

Hardware Realization of Multilayer Neural Networks Using Memristor Bridge Synapses

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ABSTRACT

The memristor, theoretically predicted by Leon O. Chua in 1971 as the fourth fundamental two-terminal circuit element, establishes a constitutive relationship between electric charge and magnetic flux. Its practical realization was reported by Strukov *et al.* in 2008 using a nanoscale TiO₂ device, demonstrating resistance switching associated with the migration of oxygen vacancies within the oxide layer. One of the most promising applications of memristors is their use as artificial synapses. In conventional neuromorphic circuits, synaptic weights are generally represented by stored digital or analog values and require separate memory and multiplication circuitry. In contrast, a memristor can simultaneously provide programmable memory and analog signal modulation through its resistance state. The continuous or multilevel memristance of a device can therefore be used to represent synaptic weights, while an applied input voltage produces a corresponding weighted current or voltage. However, a single memristor naturally represents a non-negative conductance, creating difficulties in implementing signed neural-network weights, particularly negative and zero synaptic weights.

From the investigation of the relationships among flux, charge, and memristance of diverse composite memristors and analysis of the characteristics of complex memristor circuits, it was found that memristor bridge synapses provide an effective solution to this limitation. The bridge architecture employs four memristors in a back-to-back configuration, where the differential conductance between the two branches determines the effective synaptic weighting. This arrangement enables the realization of positive, negative, and zero synaptic weights while retaining the compactness and non-volatility of memristive devices.

A further challenge is the implementation of neural-network training directly in hardware. Although back-propagation provides an efficient software learning mechanism, its hardware realization requires gradient calculation, error propagation, and additional computational resources, which can significantly increase circuit complexity. On the other hand, the Random Weight Change (RWC) algorithm provides a hardware-friendly learning strategy based on iterative trial-and-error weight modification. Accordingly, this work investigates a hardware-oriented neuromorphic architecture based on TiO₂ memristor bridge synapses and RWC learning. The proposed approach considers the electrical behavior and programmable weighting characteristics of bridge-connected memristors and their integration into multilayer neural-network structures. Positive, negative, and zero synaptic operations are realized through differential memristive states, while electrical pulses provide a mechanism for weight programming and signal processing. The RWC learning architecture is subsequently employed to demonstrate circuit-based adaptation of the synaptic weights. Previous studies have shown that, despite requiring more iterations than back-propagation, RWC can provide substantially faster learning when implemented directly in hardware, with reported learning times

approximately two orders of magnitude lower than software-based counterparts. The proposed approach therefore demonstrates the potential of memristor bridge synapses to provide analog synaptic weighting, and learning within a compact hardware platform, offering a promising route toward energy-efficient and high-density neuromorphic computing systems.

Index Terms— *Memristor; TiO₂ memristor; Memristive device; Neuromorphic computing; Memristor bridge synapse; Multilayer neural network; Random Weight Change (RWC); Hardware learning.*

BIBLIOGRAPHY

- C. Yang, C. H. Kim, S.P. Adhikari, L. O. Chua, "Circuit-Based Neural Network with Hybrid Learning of Backpropagation and Random Weight Change Algorithms," *Sensors* vol. 17, no. 16, 2017.
- F. Aguirre, A. Sebastian, M. Le Gallo, W. Song, T. Wang, J. J. Yang, W. Lu, M.-F. Chang, D. Ielmini, Y. Yang, A. Mehonic, A. Kenyon, M. A. Villena, J. B. Roldán, Y. Wu, H.-H. Hsu, N. Raghavan, J. Suñé, E. Miranda, A. Eltawil, *et al.*, "Hardware implementation of memristor-based artificial neural networks," *Nature Communications*, vol. 15, no. 1974, 2024.
- H. Kim, M. P. Sah, C. Yang, T. Roska, and L. O. Chua, "Memristor bridge synapses," *Proceedings of the IEEE*, vol. 100, no. 6, pp. 2061–2070, 2012.
- L. O. Chua, "Memristor—The missing circuit element," *IEEE Transactions on Circuit Theory*, vol. 18, no. 5, pp. 507–519, D. B. Strukov, G. S. Snider, D. R. Stewart, and R. S. Williams, "The missing memristor found," *Nature*, vol. 453, pp. 80–83, 2008.
- R. K. Budhathoki, M. P. D. Sah, C. Yang, H. Kim, and L. Chua, "Transient behaviors of multiple memristor circuits based on flux charge relationship," *International Journal of Bifurcation and Chaos*, vol. 24, no. 2, Art. no. 1430006, 2014.
- R. K. Budhathoki, M. P. Sah, S. P. Adhikari, H. Kim and L. Chua, "Composite Behavior of Multiple Memristor Circuits," in *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 60, no. 10, pp. 2688-2700, Oct. 2013.
- S. P. Adhikari, H. Kim, R. K. Budhathoki, C. Yang, and J. M. Kim, "Learning with memristor bridge synapse-based neural networks," in *Proceedings of the 14th International Workshop on Cellular Nanoscale Networks and their Applications (CNNA)*, 2014.

Speaker's short biography:



Ram Kaji Budhathoki received the B.E degree in Electrical and Electronics Engineering from Kathmandu University, Nepal in 2001. He received the M.E. degree in Computer Engineering from Pokhara University, Nepal in 2009 and the Ph.D degree in Electronics and Information Engineering from Chonbuk National University, Jeonju, South Korea in 2015. He is currently working as a Professor in the department of Electrical and Electronics Engineering at Kathmandu University, Nepal. He has worked in the same department at Kathmandu University as an Associate Professor from 2018 to 2024. He had worked as a full time faculty (Teaching Assistant to Associate Professor) at Nepal Engineering College, Nepal from Aug 2002 to June 2018. He is a senior member of IEEE. Dr. Budhathoki has been editorial board member of several international journals and technical program committee member of several international conferences. His current research interests include circuit design, analysis of memristor and memristive systems, IoT, neural networks and electronics in agriculture.